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Atty. Dkt. No. 039153-0433 (C167596-CIP)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: Sander, et al.

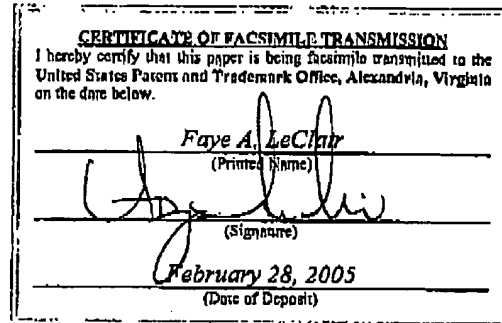
Title: MINIMIZING TRANSISTOR  
SIZE IN INTEGRATED  
CIRCUITS

Appl. No.: 10/042,732

Filing Date: 4/25/2001

Examiner: Thanh T. Nguyen

Art Unit: 2813



**AMENDMENT AND REPLY UNDER 37 CFR 1.111**

Mail Stop **AMENDMENT**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

This communication is responsive to the Non-Final Office Action dated November 26, 2004, concerning the above-referenced patent application.

The listing of claims which begins on page 2 of this document.

Remarks/Arguments begin on page 6 of this document.

001.1744893.2

Application No. 10/042,732